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10EC009

M.Tech. Degree Examination, June 2012
Advances in VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Bring out differences between CMOS and BICMOS. **(04 Marks)**

b. Explain the operation of MESFET under different gate bias conditions with the help of neat figures. **(08 Marks)**

c. An n-channel si JFET has $N_a = 5 \times 10^{18}$ cm^{-3}, $N_d = 10^{15}$ cm^{-3}, a (half the channel width) = 1.5 μm, L = 10 μm, (Z/L) = 5. Assume $n_i^2 = 10^{20}$, relative dielectric constant 11.8, free space dielectric constant = 8.85×10^{-14} F/cm, $q = 1.6 \times 10^{-9}$ C, $\mu_n = 1300$ cm^2/vs.
Determine:
i) Built in voltage ii) Pinch-off voltage. **(08 Marks)**

2 a. Mention three categories which correspond to three different sources that alter MOSFET device performance as channel length decreases. Discuss any one in detail. **(10 Marks)**

b. Calculate threshed voltage for a realistic n-channel MIS device given the following data.
$N_a = 10^{17}$ cm^{-3} $Q_i = 10^{11}$ q/cm^2
$\phi_{ms} = -0.95$ v d = 20 nm.
Comment on threshold voltage. **(10 Marks)**

3 a. With help of neat sketch, explain the construction and working of carbon nano tube FET. List out its advantages. **(10 Marks)**

b. Mention and discuss the advantages of features of molecular materials which can be applied to biomolecules. **(10 Marks)**

4 a. What are super buffers? Explain operation of NMOS super buffer CKT with neat figure and stick diagram. **(10 Marks)**

b. With help of neat CKT, explain general 2 variable functional block for six o/p logic functions 2 i/p NMOS functional block. **(10 Marks)**

5 a. Derive an expression for propagation delay in terms C_L, C_g for 2 i/p NOR gate driving a super buffer for different fanout values. **(12 Marks)**

b. Write short notes on NMOS super buffer. **(08 Marks)**

6 a. Realize static ADI gate to realize $y = \overline{(AB + CD)}$ using NMOS and CMOS technology. **(10 Marks)**

b. Realize NAND implementations of NMOS 4:1 mux using depletion mode transistor and A dynamic CMOS 4:1 mux using a clocked precharge pull-up. **(10 Marks)**

7 a. Using Gajski-kuhn y chart. Describe integrated circuit in terms of 3 domains. **(10 Marks)**

b. Discuss structured design techniques in detail. **(10 Marks)**

8 Write short notes on any two of the followings:

a. Barrel shifter

b. Full custom design

c. Defect tolerant computing.

d. Scaling theory. **(20 Marks)**

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